# WBS 6.4.2.1
# Liquid Argon Calorimeter Testing

Tim Andeen

University of Texas at Austin

NSF Conceptual Design Review of the U.S. ATLAS HL-LHC Upgrade
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# Bio-Sketch / Institute Overview

- Tim Andeen:
  - Assistant Prof. at UT-Austin, Fall-2015
  - ATLAS member since 2008
    - Fellow, CERN, 2008-2010; Postdoc, Columbia University, 2010-2015
  - LAr Phase 1 Upgrade Role:
    - Led testing of a new radiation-hard, high-speed Analog-to-Digital Convertor (ADC) for Phase 1 Front-end upgrade (LTDB).
    - Searches for exotic new physics.

- UT-Austin
  - New ATLAS institution as of Feb, 2016 (previously 3 years as sub-institute of U. Chicago).
  - 2 professors (Peter Onyisi, TA)

# Outline

- This talk – testing and performance of ASICS (ADC) and FEB2 boards.
  - ADC testing
    - Need and description
    - Work required – Performance and Irradiation
    - Experience from Phase 1
  - FEB2 testing
    - Need and description
    - Experience from original FEB
      - HASS testing
      - Workflow
    - [System Integration - DOE scope]

# ASIC Testing

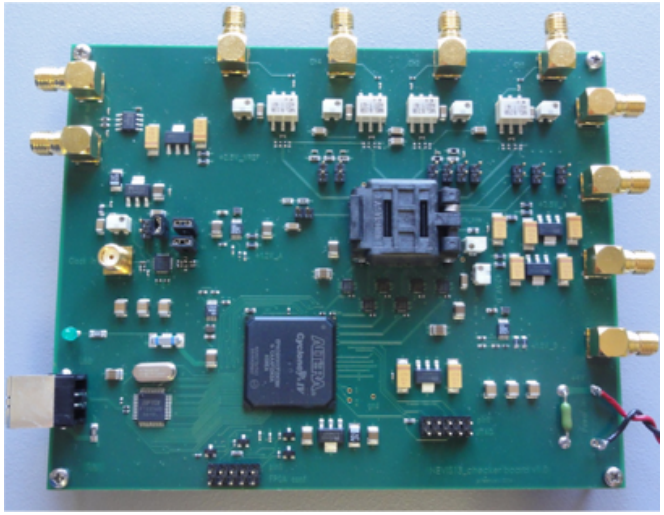
- Verify ADC functionality:
  - For novel ADC designs it is critical to verify performance of individual test chips and large batches. Can also provide feedback to R&D effort.
- Work split between performance testing (university) and irradiation testing (test beam facility).
  - Performance testing:
    - Precision, dynamic range, power consumption, noise and cross-talk, reliability (QA/QC).
  - Irradiation testing:
    - TID, NIEL, and SEE/SEU testing

# Characterizing ADC

- Sine-wave FFT method –industrial standard for ADC characterization.
- Typical parameters (figures of merit) for ADC characterization.
  - SFDR - Spurious Free Dynamic Range - Worst spurious value in the frequency spectrum w.r.t. the signal. For characterization the input signal is as close to the full range as possible.
  - SINAD - SIgnal to Noise And Distortion - The ratio of the signal amplitude to the root-sum-square of all spectral components, including harmonics. Generally, the SINAD gives the best indication of the ADC performance.
  - ENOB - Effective Number of Bits - Typically calculated by ~(SINAD-1.76dB)/6.02.
  - INL/DNL - Integral/differential non-linearity - Difference between an actual step width and the ideal value (DNL) and the deviation of the actual transfer function from a straight line (INL).

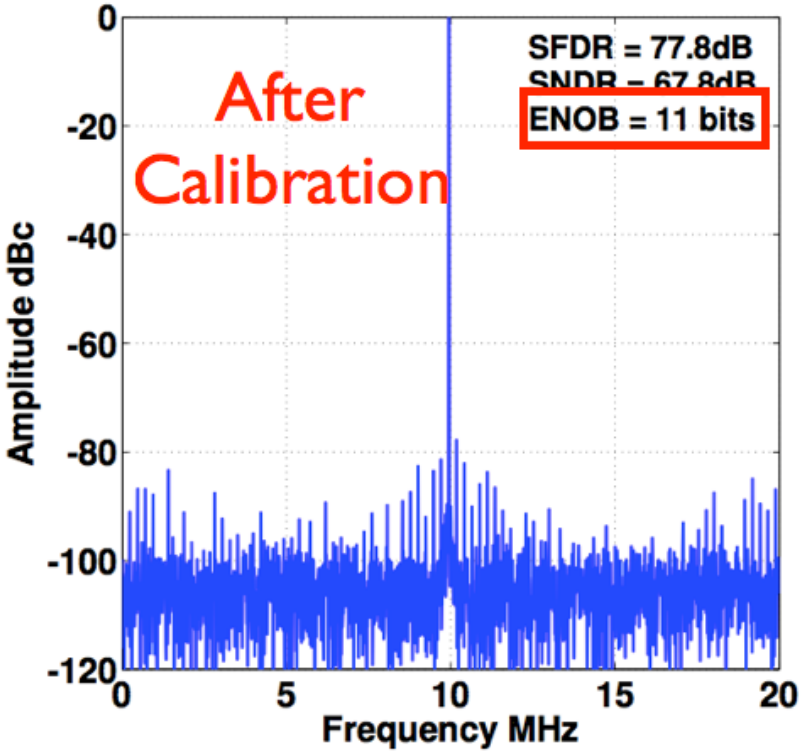
# ADC measurements

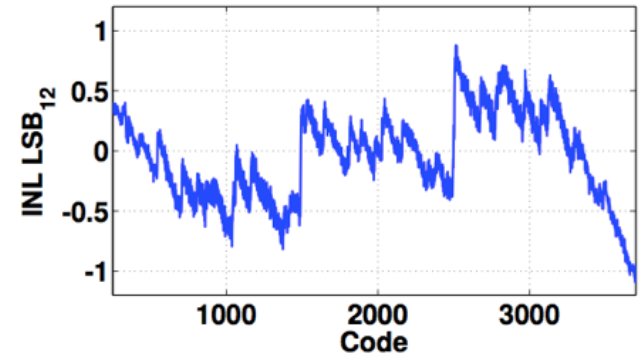
- Work involves performance measurements, as well as power consumption, noise and crosstalk between channels, prototype integration tests, and reliability (large batch testing), which will all be done at the university.
- Requires a test bench and PCBs (w/FPGA) designed to control/readout chip as well as DAQ and analysis software (physicist effort).

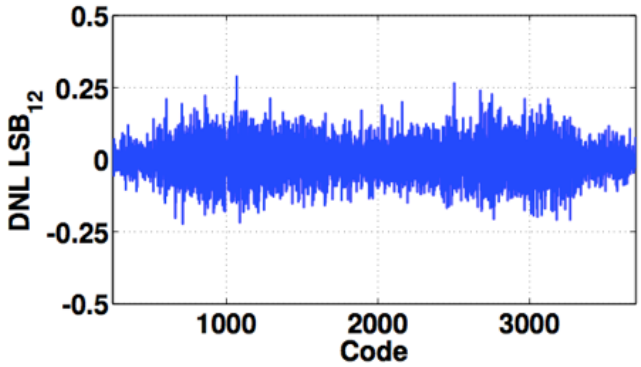


# ADC Performance – Phase 1

- Example: Performance tests of ADC design for Phase 1.




- Experience from Phase 1 upgrade provides a guide for estimating effort.

# Electronics Radiation Tolerance

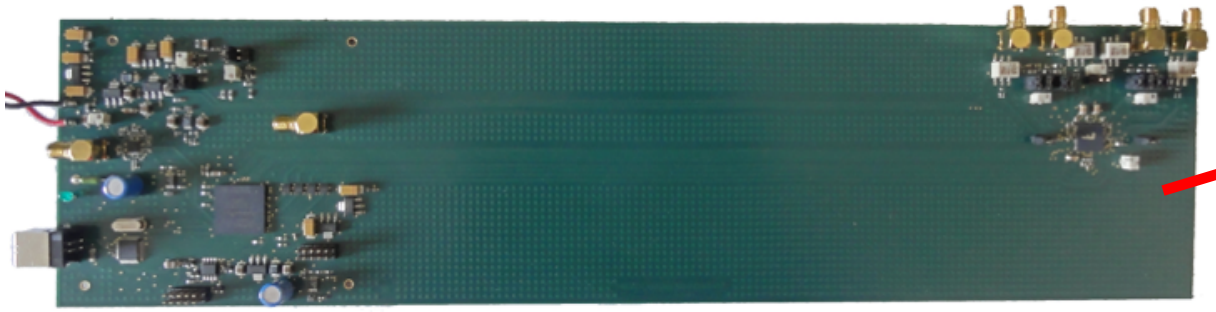
- ATLAS policy for HL-LHC radiation tolerances.
- Criteria set for three areas of concern:
  - TID (Total Ionizing Dose): cumulative over HL-LHC running
  - NIEL (Non-Ionizing Energy Loss): equivalent fluence of neutrons
  - SEE (Single Event Effect): transient effect, measured *in situ*.

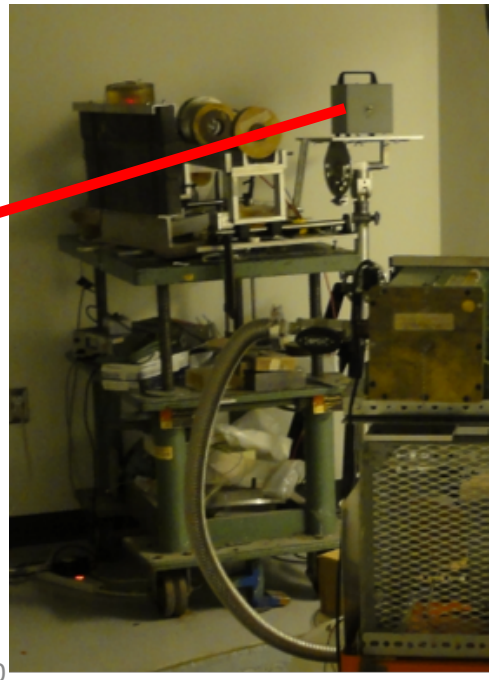
**Table 14.** Radiation tolerance criteria of the LAr electronics for operation at HL-LHC for a total luminosity of 3000 $fb^{-1}$, including safety factors for background estimation, given in brackets. For COTS, an additional safety factor of 4 is included in case of production in unknown multiple lots. Furthermore, the ATLAS policy specifies annealing tests that allow reducing the enhanced low dose rate safety-factor to 1, which currently is set to 1.5 for ASICs and 5 for COTS.

| | TID [kGy] | | NIEL [$n_{eq}/cm^2$] | | SEE [$h/cm^2$] | |
|---|---|---|---|---|---|---|
| ASIC | 0.75 | (2.25) | $2.0\times10^{13}$ | (2) | $3.8\times10^{12}$ | (2) |
| COTS (multiple lots) | 9.9 | (30) | $8.2\times10^{13}$ | (8) | $1.5\times10^{13}$ | (8) |
| COTS (single-lot) | 2.5 | (7.5) | $2.0\times10^{13}$ | (2) | $3.8\times10^{12}$ | (2) |
| LVPS (EMB and EMEC) | 0.58 | (30) | $9.2\times10^{12}$ | (8) | $2.4\times10^{12}$ | (8) |
| LVPS (HEC) | 0.17 | (2.25) | $4.7\times10^{12}$ | (2) | $2.7\times10^{11}$ | (2) |

# Radiation measurements

- Work involves irradiation testing at test-beam facilities (e.g. protons at Mass. Gen. Hospital, neutrons at LANCE facility at Los Alamos) for measurement of TID, NIEL and SEE/SEU sensitivity.
- Requires specially designed PCBs + FPGA software as well as remote DAQ and analysis software.





# ADC Irradiation– Phase 1

- Phase 1 ADC radiation tests with proton beams digitizing at 40 MHz.
- Guided by Phase 1 experience for estimates of effort required.
- Tools from Phase 1 will be adapted to HL-LHC.

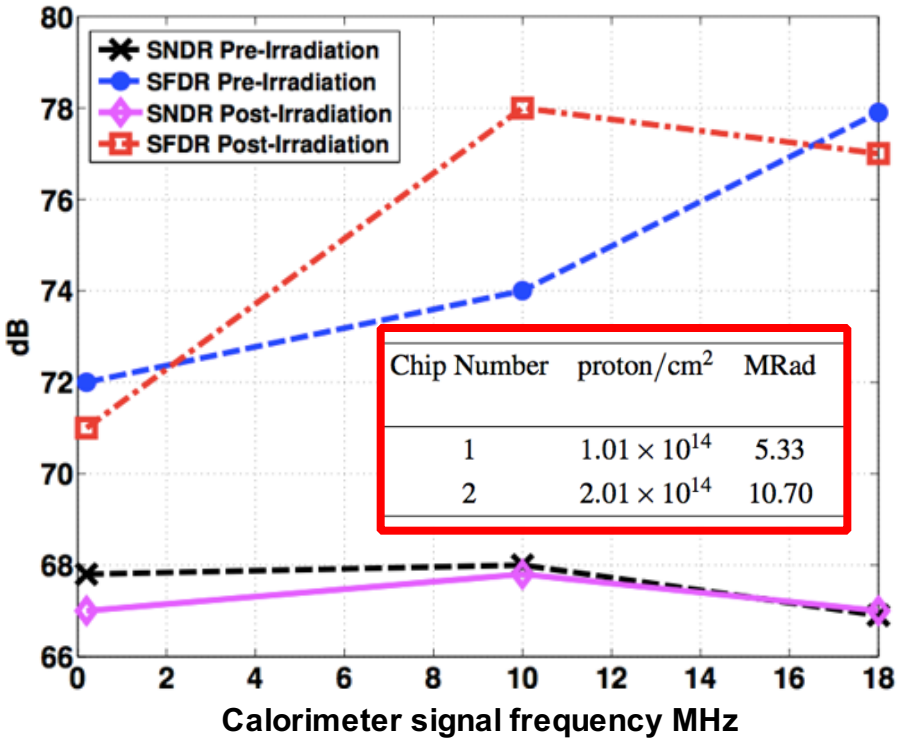


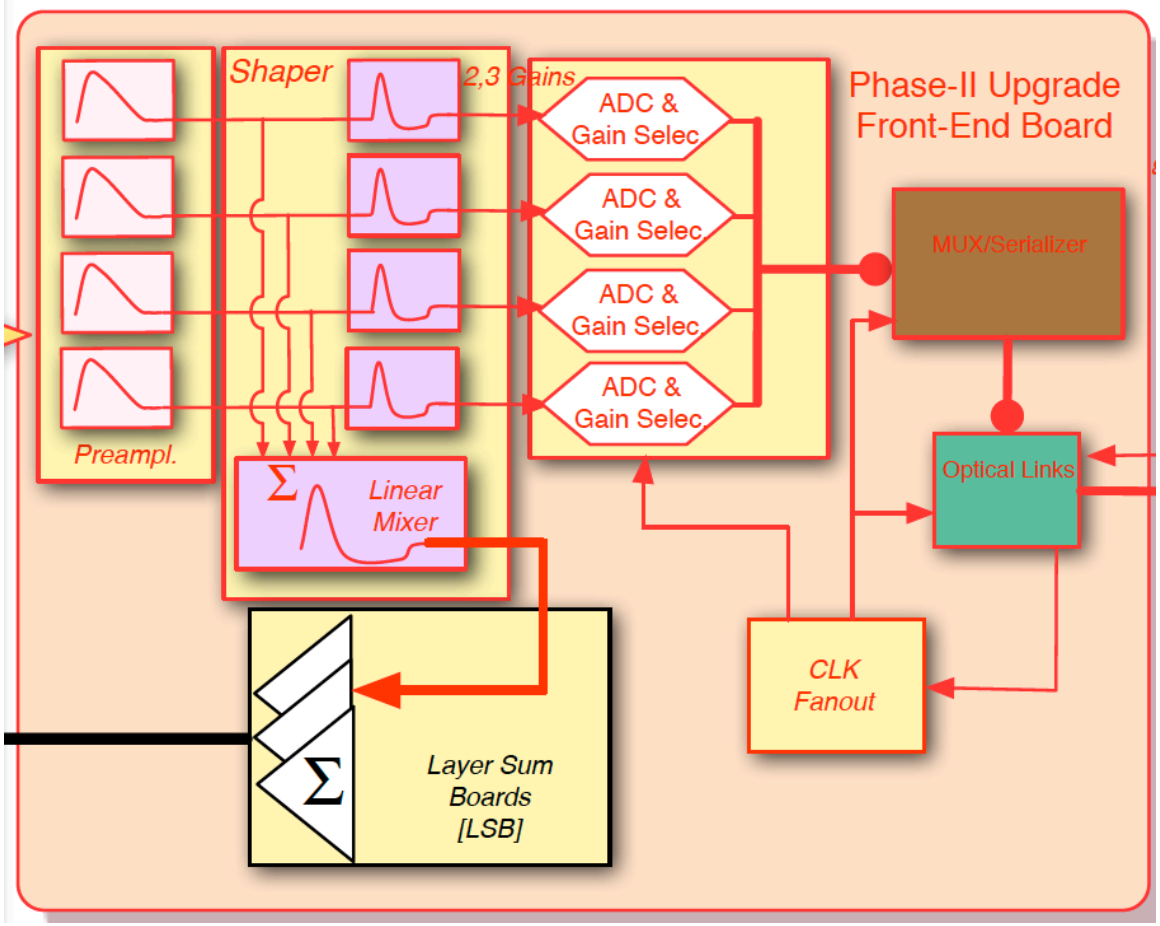

Table 2: Measurements of ADC SEE performance in a 227 MeV proton beam.

| Chip No. | Rate [$10^8$proton/cm$^2$/s] | Dose [kRad] | SEFI | SEU (analog) | SEU (digital) | SEE | Cross section (w/analog errors) [$10^{-12}$ cm$^2$] |
|---|---|---|---|---|---|---|---|
| 3 | 19.0 | 101 | 0 | 8 | 1 | 12 | 0.6 ($5.1 \pm 1.8$) |
| 3 | 76.0 | 283 | 0 | 41 | 2 | 43 | 0.6 ($9.8 \pm 1.5$) |
| 4 | 18.6 | 203 | 1 | 10 | 0 | 11 | 0.3 ($3.5 \pm 1.1$) |

# FEB2 Testing

- With custom ASICs, plus the mixed analog-digital nature of the FEB2, develop custom test setup and procedures.

- Many Radiation-tolerant (65 nm) ASICs
  - Preamp/shaper (BNL, U Penn)
  - 40 MHz ADC (Columbia)
  - 10 Gbps Serializer (SMU)
  - VCSEL array driver (SMU)



# HASS Testing

- Custom test stands will be developed. Several stages of testing are planned.
  - Initial, single FEB testing: Powering, configuration and readout of individual chips, triggering readout of FEB.
  - Highly Accelerated Stress Screening (HASS): A test stand will be installed in an environmental chamber. Multiple FEBs at once will be subjected to a series of thermal cycles (verifies cold solder joints).

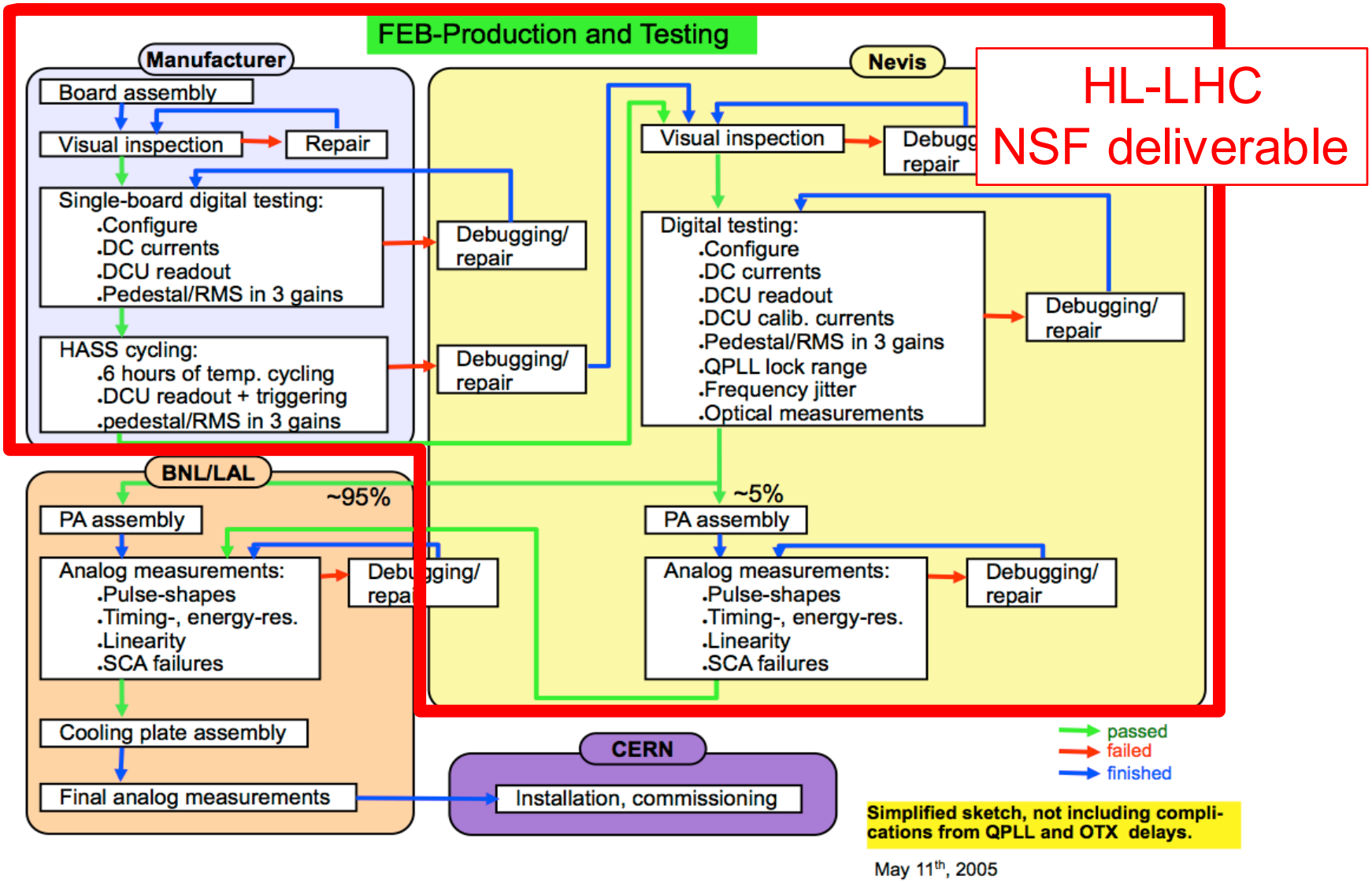
2005 HASS testing

# FEB Testing

- Parameters measured in original FEB testing.
- Anticipate a similar (where appropriate) table for FEB2.
- For FEB2 we will have clearly defined acceptance windows.
- Success is defined in-house, without need of external testing.

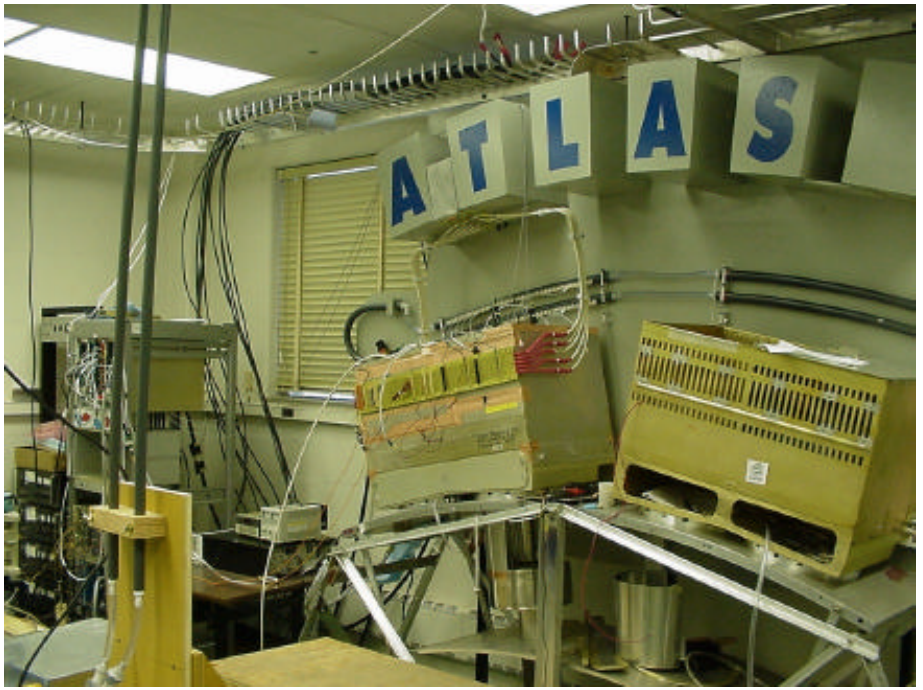
| Parameter Type | Measurement | Units | Min. Value | Max. Value |
|---|---|---|---|---|
| Pedestals | Mean | ADC counts | 880 | 1080 |
| | RMS (w/o preamps) | ADC counts | 0.5 | 1.5 |
| Clock Quality | Jitter | ps | 5 | 30 |
| | Lower Edge of Lock Range | kHz | $f_{LHC}$ - 6 | $f_{LHC}$ - 2 |
| | Upper Edge of Lock Range | kHz | $f_{LHC}$ + 2 | $f_{LHC}$ + 6 |
| | Width of Lock Range | kHz | 5 | 11 |
| Optical Output Quality | Data-dependent Jitter | UI | 0.01 | 0.18 |
| | Average Optical Power | dBm | -10 | -0.01 |
| | Extinction Ratio Opt. Output | dB | 10 | 30 |
| DCU Quality | Current Source | $\mu$A | 10 | 35 |
| | Temperatures (uncalibrated) | degC | 15 | 35 |
| DCU Voltage Monitoring | 3.3 V SCA VDDD | V | 3.2 | 3.4 |
| | 3.3 V SCA VDDA | V | 3.2 | 3.4 |
| | 2.5 V dig. | V | 2.4 | 2.6 |
| | -1.7 V SCA VSS | V | -1.875 | -1.6 |
| | 3.0 V preamps | V | 2.9 | 3.1 |
| | -3.0 V shaper VSS | V | -3.3 | -2.7 |
| | 4.5 V shaper VDD | V | 4.40 | 4.65 |
| Power Consumption | Current +6 V dig. | A | 2.06 | 2.28 |
| | Current +11 V (w/o preamps) | mA | 2 | 7 |
| | Current +6 V analog | A | 4.23 | 4.53 |
| | Current +4 V | A | 2.6 | 2.9 |
| | Current -4 V | A | 4.84 | 5.36 |
| | Total Power Dissipation | W | 67.4 | 74.0 |

# FEB Production - 2005



# System Integration: DOE Scope

- **Provide for informational purposes : DOE Scope.**
- Important to test all aspects of FEB2 in integrated system before launching production of 1600 boards.
  - Frontend Crate System Test, performed to validate the FE system integration and overall performance of the various FE crate boards (including FEB2)
  - Validation and final analog tests of 50% of the FEB2 boards
  - Integration and combined system test of FE and BE electronics




- **The equivalent tests were performed at BNL during the original ATLAS construction**

# Summary

- Testing of ASICS and FEB2 critical for success of LAr electronics upgrade.
- Plans for testing ASICS (ADC) and FEB2:
  - Build on experience from original construction and Phase 1
  - Required little external input required (success defined and determined in house).
- University groups involved (Columbia, UT Austin) are experienced at ASIC and board testing, including from original construction and from Phase I upgrade.

# Additional Material

# Summary Cost Table

| 6.4.x.1 LAr FE Electronics | | | | | | |
|---|---|---|---|---|---|---|
| | | Labor | Labor | M&S | Travel | TOTAL |
| WBS | Description | FTE | Ayk$ | Ayk$ | Ayk$ | Ayk$ |
| 6.4.x.1 | LAr FE Electronics | 34.9 | 5,370 | 4,948 | 95 | 10,414 |
| | Instr. Physicists | 5.6 | | | | |
| | Engineers | 14.9 | | | | |
| | Techs | 13.4 | | | | |
| | EE PhD Students | 1.0 | | | | |
| | | | | | | |
| 6.4.1.1 | LArFE_Columbia | 29.9 | 4,947 | 4,816 | 55 | 9,818 |
| | Instr. Physicists | 5.6 | | | | |
| | Engineers | 12.4 | | | | |
| | Techs | 10.9 | | | | |
| | EE PhD Students | 1.0 | | | | |
| | | | | | | |
| 6.4.2.1 | LArFE_UTAustin | 5.0 | 423 | 133 | 40 | 596 |
| | Instr. Physicists | - | | | | |
| | Engineers | 2.5 | | | | |
| | Techs | 2.5 | | | | |
| | EE PhD Students | - | | | | |

# Cost Estimation

- Given the similarity of our HL-LHC deliverables to our previous ATLAS responsibilities, cost and manpower estimates are mostly based on our experience with either the original ATLAS construction project or the ongoing ATLAS Phase I upgrade project.
  - ASIC Testing: Estimated based on Phase 1 ADC development for LTDB.
  - FEB Testing: Estimated based on original FEB construction, and adjusted to reflect differences between FEB and FEB2 boards.

# Glossary

- FEB – Front End Board for Liquid Argon (LAr) Calorimeter readout.
- Phase 1 - 2019-2020 detector upgrade installation (trigger path for LAr Calorimeter.
- HASS – Highly Accelerated Stress Screening